# Integration of a Fabrication Process for an Aluminum Single-Electron Transistor and a Scanning Force Probe for Tuning-Fork-Based Probe Microscopy

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Abstract—In this paper, we report on the integration technique and fabrication of a scanning probe interrogating the location of charges and their tracks inside quantum devices. Our unique approach is to pattern the charged sensor into a high topography micromechanical structure. A single-electron transistor (SET) is directly integrated onto the microfabricated cantilever that extends out from the body of a scanning force microscope (SFM) probe of standard dimensions. In a novel tactic and by reversing their traditional roles, a tuning fork (TF) completes the probe to provide the self-actuating and self-sensing qualities necessary for an oscillatory force sensor. We show sharp edges on the Coulomb diamonds, indication that the SET fabrication step yields devices of high quality. We demonstrate topographical scans with this probe. All stages of the fabrication process are executed on batches of probes which is an essential step away from the time-consuming and individual preparation of other implementations. It opens the door to a more reproducible and large volume [2009-0280] production.

Index Terms—Electron beam lithography (EBL), micromachining, microscopy, nanolithography, single-electron transistor (SET).

#### I. INTRODUCTION

**S** INGLE-ELECTRON transistors (SETs) are very sensitive electrometers with a sensitivity reaching down to fractions of the elementary charge [1]. They are considered the best device for charge detection in terms of charge sensitivity [2]. If an SET can be positioned precisely and closely to an electronic device in operation, i.e., one that has charges moving through it, then information on the electronic transport inside the device can be obtained. This resembles charge spectroscopy, however

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not the probe but the device provides the spectrum of energies of the charges under investigation.

The first time an SET was used as a sensor and positioned by a scanning probe microscope (SPM) was to detect on its metal island the change in electrically induced charge caused by the localized charges at or near the surface of a semiconductor that was scanned [3]. The SET was fabricated onto a conically tapered glass fiber by means of three thin aluminum evaporations and the fiber was positioned using a non-contact scanning probe microscopy (NC-SPM) probe stage.

### II. MOTIVATION

The straightforward evolution of this probe concept is first, to fabricate an SET directly on an SPM probe so that the assembly step disappears and second, to use a batch fabrication approach to obtain large volumes of probes. Those are the two goals that we set ourselves.

Our probe is aimed at basic research to interrogate the location of charges and their tracks inside quantum devices. Therefore, it has to operate at cryogenic temperatures and without any optical readout because the traditional method of detecting a laser beam reflected off a deflected cantilever [4] would cause scattered light. This light could either disturb the device under observation, or disturb the SET detector, or could heat up parts of the cryostat which reabsorb the light. Inspired by scanning gate microscopy at low temperatures [5], we decided to base the probe's z-axis feedback on a TF and to integrate or combine it with an SET to address the first goal. A versatile charge detection method is Kelvin Probe Force Microscopy [6] and it is used in comparable non-optical readout environments [7]. The charge under investigation must apply an electrostatic force on the probe in order to be detected. In comparison, the work to be furnished by a charge to change the current in an SET is much lower. This non-invasiveness is why SET are used to observe systems which are easily perturbed. A handicap of "one probe at a time" fabrication methods is that very small process variations in deposition, etching, gluing, and so forth add up to make that individual probes differ often significantly from each other in physical characteristics. This makes comparison of measurement results coming from a single sample, but done with different probes, difficult or impossible. Batch processing does not eliminate probe-to-probe differences by such process variations, but makes that they are not caused by processing time dependent parameters, such as

evaporation rates, but caused by the relative position of the probes on the handling wafer such as axial offset to a deposition source. Our group has batch fabricated TF-based SPM probes in the past [8]–[10] and with the aforementioned advantages of batch fabrication in mind, we approached the second goal.

Driven by similar ideas, two groups managed to fabricate SET intended for such SPM [11], [12], but their devices did not survive the reactive ion etch (RIE) release step that cuts through the substrate, positioning the devices at the end of a sharp cantilever. The first successful fabrication of an SET placed at the tip of a non-contact scanning force microscopy (NC-SFM) [13] was realized in a batch fabrication and wafer level oriented approach where SETs were fabricated on the edge of a Si<sub>3</sub>N<sub>4</sub> membrane protruding from a Si chip. The chips were broken out off the wafer and attached abaxially oriented to the distal end of one prong of a TF. The SET showed Coulomb blockade and the tip was used in typical NC-SFM manner to produce topographical scans.

Augmenting a TF by gluing a chip containing a sensor creates probe-to-probe differences caused by the final location and orientation of the chip-with-sensor relative to the TF prong end. Our approach differs in that we do not augment a TF but we fabricate a monolithic chip, into which we insert a TF. This way, the sensor orientation or location with regard to the probe body is unchanged by the pairing with the TF. The TF contributes only as an oscillatory force sensor and not as an mechanical infrastructure.

### III. DESIGN, FABRICATION AND CHARACTERIZATION

# A. Overview

We present the patterning of a nanometer-scale device onto a micrometer-scale fabricated substrate and inserting into the latter a TF in a novel way. We employ electron beam (e-beam) lithography (EBL), evaporation, and liftoff to define an SET, and photolithography, potassium hydroxide (KOH) wet etching, and reactive ion etching (RIE) to define the holding chip. The process to fabricate the SET employs the double angle Niemeyer-Dolan evaporation technique [14], [15]. A resist stack was exposed with an EBL system to produce a shadow mask. Resistively heated thermally evaporated Al was oxidized in a time and pressure controlled way followed by a second Al evaporation step at a different inclination angle. The overlap of the two evaporation steps defines the tunnel junction area. The SET device's functionality was successfully tested in a pumped <sup>4</sup>He and in a <sup>3</sup>He cryostat for normal conductive and superconductive states. The probe was used for topography scans. The batch process allowed producing many probes with short lead time.

#### B. Principle of Sensor Operation

When an electron passes through a tunnel barrier of capacitance C, the change in charge  $\Delta Q = e$  results in a voltage buildup of  $\Delta V = e/C$  across the barrier, which makes it energetically unfavorable for any further electrons to tunnel. This situation is the Coulomb blockade (CB) of single-electron tunneling, where the current anomalously stays at zero for bias voltages of  $|V| \leq e/2C$ . To be able to observe CB, two conditions must be met. First, the thermal activation energy  $E_{\rm T} = k_{\rm B}T$  must be smaller than the barrier's charging energy  $E_{\rm C} = e^2/2C$ . This constrains the operating temperature. Second, the uncertainty on the energy of the electron, the quantum energy fluctuations  $h/\tau = h/RC$ , must be less than the  $E_{\rm C}$ , which imposes on the barrier resistance  $R_{\rm t} > R_{\rm K} = h/e^2 =$  $25.8 \ {\rm k}\Omega$ .

An SET is a single electron charging effect-based device, first proposed in [16] and first realized in [17]. Since then, several successful implementations of the same principle have been demonstrated [18]–[21]. In brief, two tunnel barriers are connected in series defining a small island between them. This suppresses the quantum-mechanical uncertainty of the electron location. A third electrode, the gate, is capacitively coupling to the island. Above conditions for observation of single electron charging effects must be met. A bias voltage is applied across the two tunnel barriers. An electron on the island may tunnel off it, if the barrier is not in CB, which is determined by the voltage applied to the gate electrode. Then the empty level on the island allows an electron to tunnel through the other barrier onto the island, again given that this barrier is not in CB. Then the cycle resumes. A small change in the voltage applied to the gate electrode changes the polarization charge the gate exerts on the island (by fractions of the elementary charge), which may move the SET from a conductive state into CB and vice versa.

Given that an SET is very sensitive to a change in charge, the scanning of an SET over a sample allows mapping the change in charge or the change in charge distribution. The change in the gate electrode polarization is measured by the change in current in the SET. In summary, the current in the scanning SET changes because the capacitive coupling between the gate electrode and charges in the sample changes; the sample works as an additional SET gate electrode.

### C. Principle of Probe Operation

TF-based resonators have been used for tapping mode but are also suitable for NC-SPM mode. The change in the interaction between tip and substrate and in the simplest form, a change in substrate topography or scanning height, shifts the resonance frequency, amplitude, and phase of the tuning fork. Depending on the chosen strategy, one of these changes is used as signal for the *z*-axis feedback loop of the probe scanner. Traditionally, TF-based probes consider tips to be an add-on to the tuning fork to remedy for the poor lateral resolution of a bare prong [22]. Electrochemically sharpened W, Fe [23] and PtIr [5] wires, tips broken off the cantilever of commercial AFM probes [24], [25], tips including supporting cantilever broken off AFM commercial probes [26], were glued to one prong end, allowing to achieve a lateral resolution orders of magnitude higher than just with a prong or prong corner, and the ability to do not solely on topography, but on other parameters such as scanning gate or magnetic force measurements. The major drawback is that each probe is assembled manually one by one. The first batch fabrication process targeting to turn TF into oscillatory force sensors known to us is the definition by inclined lithography of polymer tips on one prong end [8].



Fig. 1. Concept of SPM probe: from a silicon holding chip extends a long cantilever. A sensor is patterned at its end. Completing the chip-cantilever-sensor part with a tuning fork, inserted vertically oriented from the bottom side, turns the assembly into a self-actuated, self-sensing probe. On the top side of the chip are photolithographically patterned bonding pads and electrodes continuing on the cantilever, leading to its distal end, where they connect an ebeam lithographically patterned SET. Dimensions ( $L \times W \times T$ ) chip-body: 3.5 mm × 1.6 mm × 390  $\mu$ m, extending cantilever: 2.8 mm × 75  $\mu$ m × (10 to 20  $\mu$ m), tuning fork: 3.63 mm × 0.69 mm × 0.13 mm.

Commercially available SPM probe chips have a form factor of about  $(3.5 \text{ mm to } 4 \text{ mm}) \times (1.6 \text{ mm to } 2 \text{ mm}) \times (0.4 \text{ mm to})$  $(0.5 \text{ mm})(L \times W \times H)$ . Such probe bodies feature a small protruding cantilever carrying the sharp tip, which is used to scan the surface. We aim to develop our probe according to that form factor so that it can be used in common SPM probe holders as a drop-in replacement. All silicon parts (cantilever and base) were monolithically microfabricated as a single chip and the TF was inserted from the bottom side vertically into a predefined recess (Fig. 1). The concept of bottom-side horizontally inserted TF, similar to [9], was dismissed due to the difficulty of guaranteeing the TF alignment in order to obtain good mechanical amplification on such long cantilever. The topside vertically/horizontally applied TF with SET on the bottom side was dismissed because of the important probe inclination that would be required to avoid contact of the lower part of the chip body with the sample before the sensor gets into detection range.

### D. Two Pass Scanning for Topography and Charge

The SET is very sensitive to electrical potentials and fields which is why it may be used to detect the tracks and paths of individual charges. However, if another electrical device is operated close to the SET, then the readout of its sensor signal will be meaningless or at least heavily perturbed. In this probe design, a tuning fork is used as an oscillatory force sensor to provide the signal of the *z*-axis feedback of the probe positioning and one of its prongs, coated with one of the electrodes exciting the TF, is located at a distance of 10–20  $\mu$ m away from the SET device. Therefore, the scanning for the topographic information and for the electrical potential and fields cannot be performed simultaneously.

The scanning process is split into two stages with the drawback of doubling the scan times. In a first reckoning pass, the probe is used in NC-SFM mode to map the sample surface. In a second scanning pass, this topographical information serves the scan to position the probe at a target location and height. With the probe's actuation turned off, the SET sensor yields information on the electric field at that location. While this can be done for each scan point, it is more time efficient to first scan an entire area and gather its topographical information, then in a subsequent pass, use that information to position the probe at a fixed target height for each scan point of the area, and read the SET information. This *modus operandi* is similar to the one used for magnetic force microscopy or electric force microscopy, where this is done with the intention to separate the effects of the mechanical and magnetic/electrical components of the tip-sample forces.

#### E. Probe Fabrication Process

Both the microfabrication of the Si chip-cantilever infrastructure on one side and the e-beam lithography of the SET on the other side are fabrication processes of manageable difficulty. The problems arise from the combination of the two. Once the aluminum SET is fabricated, any process step that involves charges, such as RIE or  $O_2$  plasma treatments, has the potential to destroy the tunnel junction of the SET through charge collection in the conductors, similar to the antenna effect known from deep submicrometer transistor gate oxides. Commonly employed wet process steps, such as KOH and BHF etch and also NaOH based developers, dissolve rapidly aluminum, the material the SET is made of. Dicing or sawing may mechanically stress and eventually damage the membrane the SET is patterned on. A successful process must respect the fragile nature of such device.

Fig. 2. shows cross sections of a probe in a wafer after select fabrication steps. Exact details of the fabrication process are given in Section V. Process Details. We start with a 4-in wafer and coat it with a layer of low stress  $Si_3N_4$  [Fig. 2(a)], which will serve as etch mask and as insulating substrate for the SET. The etch mask for the potassium hydroxide (KOH) etch is first patterned by photolithography and then transferred with RIE into the Si<sub>3</sub>N<sub>4</sub> layer. After the KOH wet etch [Figs. 2(b) and 3(a)], one discerns the chip body with a recess for the TF and a long extending membrane, into which the cantilever is patterned later on. The recess and membrane are much wider than necessary for a vertically inserted TF because the design is also capable to receive a horizontally inserted TF which allows for a different TF actuation principle with mechanical amplification, as demonstrated in [5] and can be done with a simple change to the RIE release mask. Using a lift-off process, Pt bonding pads and electrodes are patterned on the top side of the wafer, aligned with the KOH etched chip bodies of the backside [Figs. 2(c) and 3(b)].

The copolymer-PMMA resist stack is spun on to the wafer, which after e-beam exposure will create a suspended bridge for the dual angle evaporation of the SET. This fabrication process was developed having wafer level batch processing in mind, however the evaporator represents a bottleneck. The sample holder can be rotated to view the source at any angle, but only carries samples up to about 3.5 cm  $\times$  3.5 cm and cannot accommodate an entire 4-in wafer. Up to here, the batch fabrication is done on wafer scale but starting here, the batch size is reduced to 10 probes that fit onto a 1.9 cm  $\times$  1.9 cm



Fig. 2. Cross sections of a probe in a wafer after select fabrication steps. (a) Deposition of  $Si_3N_4$  on Silicon wafer. (b) Pattern is defined by photolithography, transferred with RIE into  $Si_3N_4$ , which then serves as etch mask for anisotropic potassium hydroxide etch. (c) Photolithographically defined Pt electrodes are evaporated and revealed with a lift-off resist process. (d) Electron beam lithography defines shadow mask for dual angle Al evaporations which produce a single electron transistor. (e) Partial release and perforation patterns are etched through the remaining membrane of Si and  $Si_3N_4$  layers that suspend the chip and cantilever. (f) The membrane flaps close to the cantilever-TF assembly is released from the holding wafer by picking it off the wafer with a pair of pliers, breaking the remaining suspending structures.



Fig. 3. Optical photographs of  $2 \times 5$  probe arrays pictured during fabrication. (a) At the back side, after KOH etch into Si, "C" shaped Si chip body can be seen, with the large membrane area to the right. (b) Pt bonding pads and electrodes patterned on the front side.

sample. Evaporation is discussed in detail in Section III-G. *SET fabrication process* and yields the SET [Fig. 2(d)].

The probe is partially released by RIE through the remaining membrane of Si and  $Si_3N_4$  layers that suspend the chip and cantilever [Fig. 2(e)] while maintaining designed points of rupture [Fig. 4(a)]. The major ones are along either side of the chip body and two minor ones at the wide area at the cantilever end. The membrane flaps close to the cantilever body are broken out [Fig. 4(b)] before applying minute amounts of glue to the end of the cantilever and base of the Si chip. When the TF is inserted, the glue spreads between the two parts by capillarity. If the flaps are not broken out beforehand, the glue



Fig. 4. Optical photographs of probe body in wafer. (a) Top side view, after RIE etched perforations and release structures through the supporting membrane. As the chip is backside illuminated, the thin membrane turns redbrown, while the perforations and releases are overexposed, hence appearing in white, cf. Fig. 2(e). (b) Bottom side view, three flaps are broken out. The cantilever is just supported by its base and the two thin bridges near the end, cf. Fig. 2(f), red dots indicate where glue is applied.

leapfrogs the release perforation and irreversibly unites lever and flaps.

## F. Tuning Fork Insertion

Tiny amounts of glue are applied with a pin to the widening at the end of the cantilever and at the base sensor area at the end indicated by red dots on Fig. 4(b). The TF insertion to the target area marked in Fig. 5(a) is surprisingly easy. The glue droplet minimizes its surface tension by minimizing overlap and gap between the sensor area at the cantilever end where it was applied [Fig. 4(b), right red dot] and the TF prong end, which results in a perfect alignment of the two. After curing, additional glue may be inserted between the C-shaped probe body and the TF base to reinforce the supporting membrane, which otherwise tends to rupture during probe manipulation. The TF turns out to be difficult to electrically connect once inserted into the recess, which is why before redesigning an additional recess on the holding chip, a shark-fin like structure was glued with insulating epoxy glue to the TF [Fig. 5(b)]. On these, support lines are drawn with conductive epoxy to allow connecting the two TF electrodes on the shark-fin that sticks out of the Si body [Fig. 5(c) and (d)]. The chip-cantilever-TF assembly is released with pliers from the holding wafer, breaking the remaining suspending structures [Figs. 2(f), 6(a) and (b)].

# G. SET Fabrication Process

This was the first time our lab attempted to fabricate single electron transistors. Initially, we omitted the scanning probe manufacturing steps and patterned just the SET on a sample chip. This allowed us to optimize for a resist system, that with an accorded and tuned e-beam exposure and adapted development step resulted in a suspended PMMA resist bridge with suitably under-etched copolymer spacer layer. The



Fig. 5. Assembly of Si chip and cantilever with TF. (a) Dotted outline of target area for TF insertion [cf. Fig. 4(c)]. (b) TF augmented by shark fins, and conductive epoxy lines. Probe with inserted TF (c) bottom view and (d) top view.



Fig. 6. SEM pictures of assembled probe. (a) Si body with extending cantilever, TF glued from below, scalebar 100  $\mu$ m. (b) Cantilever end on top of TF prong, opposite prong visible below, SET sits at apex of converging lines. Two rupture points stick out on either side, scalebar 30  $\mu$ m.

evaporator is used for the dual angle evaporation. The intermediate oxidation step is done without breaking the vacuum. The lift-off step reveals the device. The sample chips are measured at room temperature and chips with promising series resistances are bonded into a cryostat compatible ceramic chip holder and finally characterized at low temperatures. Fig. 7(a) shows a conceptual side view of a suspended PMMA bridge, with the projected inclinations that would produce overlapping Al structures. Fig. 7(b) shows a top view of mask openings in white. Fig. 7(c) shows a top view of the two traces that the mask will cast under two evaporations at distinct angles, and Fig. 7(d) finally shows a SEM micrograph of a functional SET patterned with that method.

The Achilles' heel of aluminum SET fabrication is the formation of the tunnel junctions. Al exposed to air at room temperature forms within a few seconds a 2–3 nm thick native oxide film. Al oxide growth kinetics [27] explain that the growth stops when the  $Al^{3+}$  ions can no longer tunnel from the  $Al-Al_2O_3$ interface through the oxide film to the  $Al_2O_3-O_2$  interface to meet the adsorbed O<sup>-</sup> and O<sup>2-</sup> anions. Analogously, this is the case in reverse direction anions. At this point, the oxide film is already too thick to be useful for an SET because electrons may no longer tunnel through it. To have more than a few seconds of time to control the oxide film formation, the reaction is reactant starved by very low pressure and immediately after formation and *in situ*, the  $Al_2O_3$  film is hermetically sealed with another Al film. This way, the top Al protects the  $Al_2O_3$ film from further growth due to native oxide formation and



Fig. 7. SET fabrication principle and realization: (a) side view of resist stack. Black indicates obturating suspended mask, dark grey first evaporation from top right, light grey second evaporation from top left. (b) Top view of mask, openings in white, (c) top view of two evaporations through mask under (b), under two different angles, (d) SEM picture of realized SET.

at the same time, the junction Al-Al<sub>2</sub>O<sub>3</sub>-Al is formed. The desired quality of the junction is to have a resistance higher than 25.8 k $\Omega$  to fulfill the requirement of suppressing quantum fluctuations. But the resistance does not depend exclusively on the time of exposure to oxygen at low pressure, but on other factors, such as chamber background pressure, pressure during oxidation itself, chamber and sample temperature, Al grain size of the preceding evaporation step, and Al grain size of the following evaporation step. The resistivity can be measured at room temperature but is only an indicator of how the SET will function when operated at low temperatures. The initial SET junction series resistance changes when the probes are further processed. We attribute this to changes in the film at the grain level because although protected by photoresist, the probes are exposed to NaOH-based developer which alters Al films, even if only seen in trace amounts, further but slow native oxide formation, and RIE, which may put an electrical strain on the junctions although there are no exposed electrodes that could collect charges. The SET on the sample chips were characterized electrically at room temperature by measuring the resistance  $R_{\rm T}$  of both junctions in series. Typical candidates ranged from 100–500 k $\Omega$  but devices with  $R_{\rm T} = 3 \ {\rm M}\Omega$  were also found to be functional at low temperatures.

## H. Characterization of the SET

The sample chips are initially characterized in a pumped <sup>4</sup>He system at temperatures reaching down to 1.8 K. First single charging signatures are observed below 4.5 K. However, due to thermal activation, the Coulomb diamonds have blurry boundaries which is why a <sup>3</sup>He cryostat is used to reach temperatures of 400 mK. That experiment allows to obtain very sharp Coulomb diamonds, for both normally conducting (Fig. 8(a), with magnetic flux density of B = 0.5 T applied to suppress superconductivity) and superconducting state [Fig. 8(b)]. From these diagrams were extracted junction capacitances of  $C_1 = 86.9$  aF,  $C_2 = 86.1$  aF, which indicate the island is connected by symmetrically junctions, a gate with  $C_g = 3392$ F, an



Fig. 8. Coulomb blockade diamonds of a SET. The color bars show the differential conductance  $dI_{sd}/dV_{sd}(e^2/h)$ . Inside the central, diamond shaped zones, the differential conductance is zero, and the SET is in Coulomb blockade. (a) Normal conducting state at 400 mK with magnetic flux density of B = 0.5 T applied to suppress superconductivity and (b) superconducting state at 440 mK.

island of  $C_{\Sigma} = 173$  aF, with a resulting charging energy of  $E_c = 74 \times 10^{-24}$  J = 74 yJ = 460  $\mu$ eV. The thermal activation energy  $k_{\rm B}T$  at 400 mK lies at 5.55 yJ, and equates the charging energy  $E_c$  at T = 5.36 K. In the superconducting case, the superconducting gap is at  $\Delta = 201 \ \mu$ eV, and the Josephson Energy  $E_{\rm J} = 2.36 \ \mu$ eV. At 440 mK, the SET is in  $E_{\rm J} \ll \Delta < E_c$  regime, which means that the effects due to the Josephson energy, i.e., the supercurrent, will be very faint, and the Coulomb blockade the predominant transport (limiting) mechanism inside the superconducting gap. The most striking feature in the superconducting state is that the Coulomb blockade diamond is shifted along the y-axis by  $4\Delta/e$  in either direction [Fig. 8(b)]. Both the shift of quasiparticle conduction

onset and the visible traces of subgap transport phenomena are reported in other publications [18], [28].

#### I. Patterning of the SET Onto Probe

The SET is patterned onto the probe with the membrane still intact, cf. Figs. 2(d) and 3(b). The RIE step that follows frees the probe from the membrane, cf. Figs. 2(e) and 4(a) and also in the sensor area at the cantilever end, cf. Fig. 9(a). This step has the potential to get too close to the sensor, to cut into it, or to damage it by stray charges. The distance between sensor and photoresist tip apex is about 8  $\mu$ m on Fig. 9(b) before etching. This distance could be reduced to

Fig. 9. (a) SET sensor area at end of cantilever, dark lines indicate material removed by RIE, defining area suspended from bottom and top of picture by narrow bridges, cantilever to the left. (b) Alignment of patterned leads (bright) leading to SET and the trench in the photoresist (dark) prior to RIE etch. (c) SEM micrograph of SET, annotated inset with drain (D), gate (G), source (S) and island (I), with indices for first (1) and second (2) evaporation.



about 1  $\mu$ m with careful control of mask alignment and RIE etch undercut. The closer the sensor is to the tip apex, the higher is the spatial resolution of the sensor because it is closer to the surface that it is scanning. Another benefit is that the topographical image closely matches the sensor readout. This is comparable to a known problem when aligning the optical outline of commercial cantilevers with a sample, knowing that the tip patterned on the lower side of the cantilever has a several micrometer offset and the tip position only can be guessed. The SET on the assembled probes were characterized electrically at room temperature and had comparable  $R_{\rm T}$  ranging from 100–500 k $\Omega$  as the non-integrated SET on the sample chips. The charge sensitive area of the SET is the island and to a lesser extent the gate. We expect to hover at 50 nm above the surface where the island dimension of 100 nm diameter dominates the possible lateral resolution and expect to be able to distinguish two charges in a 2DEG buried 100 nm deep and 400 nm separated from each other.

# J. Topographical Scan With Probe

We used an assembled probe to perform tapping mode in air SPM on calibration samples and to ascertain that the probe principle of vertically inserted TF is functional. At the cantilever end, the edges converge in a corner which is used in lieu of a tip. Because of that, high lateral resolution is not possible, but in return, no additional distance is introduced to keep the tip separated from the device under investigation. We wanted proof that the topographic information obtained is capable to guide the observer to a target device area of several micrometer square and that there, precise height information can be obtained. The image in Fig. 10 resolves 20 nm high structures and is a proof of probe's z-feedback concept. The scan pixel size of 120 nm is limiting the lateral resolution but sufficient to position the SET with regard to the sample device. The tip appeared to be very robust and lasted during an entire day of scanning, which is an indicator that the stress exerted by the TF oscillatory movement on the cantilever does neither exceed its mechanical limits nor the ones of the entire probe.

Fig. 10. SPM topography calibration sample, circles, 3  $\mu m$  diameter, 20 nm high, pitch 5  $\mu m.$ 

# **IV. CONCLUSION**

We have presented the fabrication of a scanning singleelectron transistor probe. We have shown successful SET operation in a cryostat under ultra high vacuum conditions, revealing the characteristic Coulomb diamonds for both superconducting and normal conducting states, which validates the SET fabrication process. We have integrated this SET fabrication process into a cantilever fabrication process. This mechanical device was successfully shown as a scanning force probe at room temperature, confirming successfully running an AFM probe at room temperature. We have proposed for this probe a two pass technique, first SPM scanning for topography then SET scanning in charge spectroscopy mode. However, the assessment of this approach at low temperatures could not be concluded which is why there is no result for this core goal.

## V. PROCESS DETAILS

The fabrication of the holding chip starts with double side polished Si wafers (crystal orientation  $\langle 100 \rangle$ , 4" diameter, ntype doped, 5  $\Omega$ cm, 390  $\mu$ m thick). They are submitted to an RCA procedure-inspired wet standard cleaning as follows. Immerse in Sulfuric acid (H<sub>2</sub>SO<sub>4</sub>) 96% at 120 °C, to which a spoonful of hydrogen peroxide (H<sub>2</sub>O<sub>2</sub>) is added immediately before use, for 10 min, to remove organic residues. Rinse in deionized water (DI H<sub>2</sub>O). Immerse in Buffered Hydrofluoric acid (BHF) composed of a 7 : 1 by volume mixture of ammonium fluoride (NH<sub>4</sub>F) 40% in water and Hydrofluoric acid (HF) 49% in water, at ambient temperature for 1 min, to remove the native oxide layer. Rinse in DI H<sub>2</sub>O. Immerse in Nitric acid (HNO<sub>3</sub>) 70% in water at 115 °C for 10 min to create homogeneous native oxide layer. Rinse in DI H<sub>2</sub>O.

A 400-nm thick low stress SiN film is grown with a low pressure chemical vapor deposition process, more precisely first 15 nm standard  $Si_3N_4$ , respecting the stoechiometric ratio,

then 370 nm low stress  $Si_xN_y$ , which is not stoechiometrically correct but causes much less tensile stress in the underlying Si layer than a  $Si_3N_4$  layer and finally another 15 nm of standard  $Si_3N_4$  to complete the sandwich. If exclusively standard  $Si_3N_4$ instead of low stress  $Si_xN_y$  would be used, then the finalized Si cantilevers would bend toward the side covered with the  $Si_3N_4$ film. The  $Si_xN_y$  film is not etch-resistant to KOH as  $Si_3N_4$ , which is why it is sandwiched between two protective  $Si_3N_4$ layers.

To promote adhesion of photoresist (PR) to the substrate surface, the wafers are dehydrated (150 °C, 15 min) and exposed to gas phase Hexamethyldisilazan (HMDS) at 150 °C, 30 Pa for 5 min. PR (Clariant AZ 1518) is spin coated (spread 3 s at 500 rpm, spin 40 s at 4000 rpm) to the backside of the wafer to obtain a 1.8  $\mu$ m thick film, then baked on a hotplate for 60 s at 100 °C. Photolithography is performed with an Electronic Visions Co. AL6 mask aligner, aiming to transfer energy of 55 mJ · cm<sup>-2</sup> to the exposed areas of the pattern, the backside KOH mask. No post exposure bake was done. Development is done by immersion for 60 s (Clariant AZ351B + H<sub>2</sub>0 = 1 + 4). Post development bake is done in an oven for 30 min at 120 °C.

The KOH mask is transferred by RIE into SiN which will serve as KOH etch mask. The time controlled RIE overetches about 200–300 nm deep into the underlying Si. The PR is removed in oxygen plasma (Tepla 300 plasma processor).

The pattern is anisotropically etched in a potassium hydroxide (KOH) solution 40% in water at 60 °C. The timed etch aims to end with the exposed areas having a remaining Si thickness of 10–20  $\mu$ m. Typical etch rates observed where below 16  $\mu$ m/h and require around 24 h etching to get through the 390  $\mu$ m wafer. Rinse in DI H<sub>2</sub>O, neutralize in hydrochloric acid (HCl) 5% in water for 20 min. Rinse in DI H<sub>2</sub>O.

After dehydrating the wafers ( $120 \,^{\circ}$ C,  $30 \,^{\text{min}}$ ), a lift-off resist (LOR) system is applied to the front side, i.e., the one not etched by KOH. The thinned down membranes of the wafer can no longer resist the suction exerted by a vacuum chuck of the spin coating system. This is why a custom built chuck is used, that holds the wafer with a gentle radial squeeze in three points of its periphery with soft Teflon screws. The bottom layer (MicroChem LOR-3B) is spin coated (dynamic dispense on spinning wafer:  $10 \,^{\circ}$  s at 500 rpm, then spin 40 s at 4000 rpm), then baked on a hotplate for 10 min at 190 °C. The top layer (Shipley S-1813) is spin coated (spread 3 s at 500 rpm, then spin 40 s at 4000 rpm), then baked on a hotplate for 1 min at 115 °C.

Photolithography is performed with above EV AL6, aiming to transfer energy of 60 mJ  $\cdot$  cm<sup>-2</sup> to the exposed areas of the pattern, the front side metal electrodes. Development is done by immersion in three baths (Clairant AZ400K), first diluted 1:4 in water for 35 s without agitation, second 1:4 in water for 10 s with agitation, third 1:8 in water for 10 s with agitation. The surface is descummed in mild oxygen plasma. Metal evaporation provides for a 100 nm thick Platinum (Pt) layer on top of 5 nm thick Titanium (Ti) adhesion layer. The liftoff process uses solvent stripper (MicroChem, PG Remover) to dissolve the LOR resist system in two baths which minimizes redeposition of removed resist, both baths for 30 min at 60 °C. Rinse in isopropyl alcohol (IPA), then DI H<sub>2</sub>O.

The SET shadow mask structure is patterned on the front side of the wafer in a dual layer resist stack. The above fabricated metalized wafers are cleaned in oxygen plasma immediately before spinning, no dehydration or adhesion promotion. The bottom layer of copolymer (MicroChem, MMA(8.5)MAA EL11, methyl methacrylate with 8.5% methacrylic acid, 11% solids in ethyl lactate), diluted with ethyl lactate to 6% solids, cleansed by syringe-top particle retention filter (Millipore Millex PTFE 0.2  $\mu$ m), is spin coated (spread 5 s at 500 rpm, spin 45 s at 2000 rpm) to obtain a 200 nm thick layer. Dry on hotplate for 90 s at 180 °C. The top layer of PMMA (MicroChem, 950K PMMA A11, polymethyl methacrylate 11% solids in anisole), diluted with anisole to 2% solids, cleansed by syringetop 0.2  $\mu$ m particle retention filter, is spin coated (spread 5 s at 500 rpm, spin 45 s at 1500 rpm) to obtain a 100 nm thick layer. Dry on hotplate for 600 s at 180 °C. The SET structures are exposed with a direct write electron beam lithography (EBL) system (Raith GmbH, Raith 150). The EBL exposure parameters were optimized in function of resist stack thicknesses, different developers, and post-liftoff analysis of evaporation results. Column parameters were voltage 10 keV, aperture 30  $\mu$ m, writefield 50  $\mu$ m  $\times$  50  $\mu$ m, working distance 6 mm. Exposure parameters were: area step size 9.6 nm, area dose 100  $\mu$ C · cm<sup>-2</sup>, single pixel line step size 1.6 nm, single pixel line dose 1000  $\mu$ C · cm<sup>-1</sup>, single dot dose 0.1 pC. Development is done for 45 s in Methyl isobutyl ketone (MIBK) + IPA = 1 + 3, rinse 30 s in IPA, then 120 s in H<sub>2</sub>O. Post development bake on hotplate for 90 s at 90 °C, with the main task to evaporate trapped water and not to harden the resist. Very mild descum of 10 s in oxygen plasma stripper, to scrub the areas where metal will be evaporated upon to.

Evaporation of aluminum is performed in a thin film deposition system (Tectra Germany, mini-coater, modular high vacuum coating system) which thanks to its modular build is augmented with an orientable support, permitting angle change without breaking the vacuum, needle valve ultra pure oxygen inlet which allows to oxidize aluminum to obtain tunnel junction without breaking the vacuum, direct temperature readout at substrate level via K-type thermocouple to avoid reaching 125 °C, where PMMA images, will round/flow, which would be fatal for the shadow mask. Thermal evaporation of Al rods done in a BN basket held by a resistively heated W-wire. Coater base pressure reaches 5e-7 mbar. During the first evaporation pressure rises to 5e-5 mbar, temperature to 80 °C, while depositing 20 nm of Al. Oxidation for typically 2 min follows at pressures around 1 mbar to reach the desired junction resistance, chamber cools down to 50 °C. The second evaporation starts at 4e-6 mbar then rises to 1e-5 mbar, temperature to 100 °C, for another 20 nm of Al. Liftoff is performed for 30 min in acetone with ultrasonic agitation at 1 MHz, followed by IPA and DI H<sub>2</sub>O rinse.

After liftoff and with extreme electrostatic discharge prevention precautions, the devices' resistance is measured (hp4155a semiconductor parameter analyzer) to obtain an indicative information of the junction health and quality. Generally observed were three bins: shorted circuits ( $\Omega$  to k $\Omega$  range), SET candidates (high tens and hundreds of k $\Omega$  to tens of M $\Omega$  range), and open circuits.

To promote adhesion of PR to the substrate surface, the wafers are dehydrated (150 °C, 15 min) and exposed to gas phase HMDS at 150 °C, 30 Pa for 5 min. PR (Clariant AZ 1518) is spin coated (spread 3 s at 1000 rpm, spin 40 s at 3000 rpm) to the topside of the wafer to obtain a 2.3  $\mu$ m thick film, then baked on a hotplate for 60 s at 100 °C. Photolithography is performed with an EV AL6 mask aligner, aiming to transfer energy of 55 mJ  $\cdot$  cm<sup>-2</sup> to the exposed areas of the pattern, the topside RIE perforation mask. No post exposure bake was done. Development is done by immersion for 60 s (Clairant AZ  $351B + H_2O = 1 + 4$ ). Post development bake is done in oven for 120 min at 85 °C. This low temperature is chosen to reduce resist flux during bake. DRIE punches through SiN and remaining Si thickness, and leaves chips suspended by bridges. SET are protected by PR film. Strip PR with acetone, rinse IPA, rinse in DI H<sub>2</sub>O.

Post-DRIE-measurement show that the resistances have slightly changed, both increased and decreased, but not by orders of magnitudes.

The contact pad location on the TF makes contacting a difficult task, once they are inserted into the probe recess, which is why a quartz shard (from a TF holding wafer), alike a shark fin, is glued with insulating epoxy glue (Robnor, Araldite, HY-991 + AY105-1 = 1 + 2) onto the TF at one of the two electrode location, then a conductive epoxy (Epotek, H20E) line is drawn on either side from two contact pads to allow for later contacting on the shard instead of the TF in the recess. Both epoxy glues were used successfully in cryostat environments.

The TF with fins are glued into the Si probe body with above insulating glue, the pits are stiffened with glue to prevent separation of probe body and cantilever during handling. Break the probes out of holding wafer using pliers.

Final resistance measurements were done before mounting in cryostat to confirm that junctions are still intact. SEM images were collected in the Raith-150 EBL system. Non-contact SPM was performed with a Veeco Metrology Group Digital Instruments MultiMode AFM. The TF resonance was controlled and detected with NanoSurf easyPLL FM Sensor controller and detector systems.

We used quartz tuning forks with  $f_0 = 32768$  Hz. One prong has following dimensions: length  $l = 2370 \,\mu\text{m}$ , thickness  $t = 220 \ \mu \text{m}$ , width  $w = 127 \ \mu \text{m}$ . When modeled as a simple cantilevered rectangular beam and taking Young's Modulus of Quartz of E = 78.3 GPa, a prong's theoretical spring constant can be estimated with  $k = Ewt^3/4L^3 = 1989$  N/m. Typical quality factors are above Q = 28000. When such a TF is operated in air, additional dampening due to viscous interaction of the vibrating prongs with air drops to 32754 Hz and Q down to about 2500. When the TF is glued into the holding chip, one prong contacts the cantilever and becomes stiffer and is loaded with mass. The TF was designed to be perfectly symmetrical and due to its insertion into the CL, it now acts as two coupled resonators. The probe's cantilever is 10  $\mu$ m to 20  $\mu$ m thick. This 5–10% contribution to the prong thickness changes the estimates for the assembled probe to k = 2302 N/m and k = 2647 N/m and the probe's resonance frequency drops to  $f_r = 31780$  Hz with a quality factor of Q = 400. When the probe is operated in vacuum,  $f_r$  raises by about 35 Hz to a final 31 915 Hz (all assembled probe values are typical).

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