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Optimization of sample-chip design for stub-matched radio-frequency reflectometry measurements

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A radio-frequency (rf) matching circuit with an *in situ* tunable varactor diode used for rf reflectometry measurements in semiconductor nanostructures is investigated and used to optimize the sample-specific chip design. The samples are integrated in a 2–4 GHz stub-matching circuit consisting of a waveguide stub shunted to the terminated coplanar waveguide. Several quantum point contacts fabricated on a GaAs/AlGaAs heterostructure with different chip designs are compared. We show that the change of the reflection coefficient for a fixed change in the quantum point contact conductance can be enhanced by a factor of 3 compared to conventional designs by a suitable electrode geometry. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4739248>]

High-frequency reflectometry measurements in semiconductor nanostructures¹ allow dispersive state readout detecting the state-dependent “quantum capacitance” of a qubit² and time-resolved charge detection measurements^{3–6} using a quantum point contact (QPC)⁷ or a single-electron transistor⁸ as charge detector. We investigate a radio-frequency (rf) matching circuit as an approach to reach higher detection bandwidths in single-shot measurements compared to dc read-out techniques.^{9–11} This was motivated by exciting experiments such as the measurement of a single electron spin by spin-to-charge conversion,¹² the measurement of full counting statistics,¹³ and single-shot readout of a spin qubit.¹⁴ In contrast to previously demonstrated rf techniques,^{3–6} we use a stub-matching approach, adopted from microwave impedance matching.^{15,16}

The basic idea of reflectometry measurements is to detect the reflection of a rf-signal depending on the load terminating the waveguide. The reflection coefficient Γ is most sensitive to changes of the load impedance Z_L if Z_L is close to the characteristic impedance Z_0 of the waveguide of 50Ω .¹⁷ The reflection coefficient is given by $\Gamma = (Z_L - Z_0)/(Z_L + Z_0)$. In the presented case, the load is a QPC integrated into a rf matching circuit. The latter consists of a waveguide stub shunted to the waveguide terminated by Z_L and is integrated on a printed circuit board (PCB). The shunt-stub circuit is *in situ* tunable which simplifies the matching procedure.¹⁸ The matching circuit design as well as the sample chip design have a large impact on the measurement performance. In this paper, we focus on the optimization of the chip design. Previous transmission measurements in GaAs/AlGaAs heterostructures point to the assumption that these results may also be important for matching frequencies lower than the 2–4 GHz investigated in this paper.¹⁹ The paper is written within the scope of time-resolved charge detection measurements. The conclusions for the design of the sample chip and the PCB, however, are more generally valid for reflectometry measurements.

In the following, we discuss the setup sketched in Fig. 1(a). A rf carrier signal is generated by a vector network analyzer (VNA) and applied to the sample via a directional coupler. Before reaching the sample, a dc component is added to the signal by using a bias tee. At the PCB, containing matching circuit and sample, the rf signal is partly reflected and afterwards amplified by 60 dB using a 2–4 GHz room temperature amplifier before reaching the input port of the VNA. Dc blocks are used to avoid ground loops. All components except for the PCB are placed at room

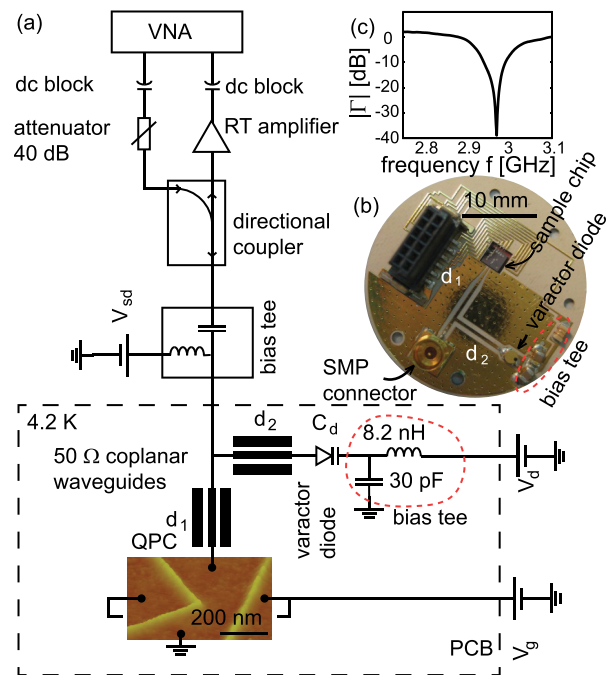


FIG. 1. (a) Experimental setup used to perform the measurements and designed for carrier frequencies of 2–4 GHz. (b) Photograph of the PCB with the two stubs terminated by a varactor diode and the QPC, respectively. Two capacitors and one inductor placed after the diode act as on-chip bias tee. (c) Absolute value of the reflection coefficient $|\Gamma|$ as a function of the carrier frequency f for a QPC conductance of $g = 3 \times 2e^2/h$.

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temperature for ease of calibration. The calibration is done in 3 steps using commercial calibration kits.²⁰

A schematic of the PCB is shown in the dashed box in Fig. 1(a) and on the photograph in Fig. 1(b). The substrate of the PCB is AD1000 (Arlon), with a dielectric constant of 10 and a roughly 17 μm thick copper layer. A thin gold coating prevents oxidation. The transmission lines on the PCB, coplanar waveguides with ground plane (CPWG), form the matching circuit and have a loss of about 3.88 dB/m at 3 GHz. The sample chip including the QPC (shown in the atomic force microscope (AFM) scan in Fig. 1(a)) is glued into a $3 \times 3 \text{ mm}^2$ recess at the end of the CPWG and connected with bond wires.

Impedance matching is achieved by a CPWG stub shunted to the 50 Ω CPWG at a distance d_1 of about $\lambda/4$ from the QPC load, where λ is the wavelength of the roughly 3 GHz carrier signal. The stub has a length d_2 of about $\lambda/4$ and is terminated by a varactor diode. The capacitance C_d of the diode is *in situ* tunable by applying a dc voltage V_d .¹⁸ A bias tee, consisting of two on-chip capacitors of 15 pF each and of an inductor of 8.2 nH, is placed on the PCB close to the diode. This provides a rf ground for the rf signal without affecting the dc voltage V_d tuning the diode's capacitance. The influence of the bias tee on the rf circuit performance is irrelevant as the diode capacitance C_d of 0.3–1.1 pF is small enough compared to the capacitance of the on-chip bias tee. The total impedance Z_L of the stub-matching circuit with integrated QPC and diode is given by the inverse of the sum of the two admittances—the one of the CPWG part from the load to the stub including the QPC Y_{d_1} and the one of the stub including the diode Y_{d_2}

$$Z_L = Y_L^{-1} = (Y_{d_1} + Y_{d_2})^{-1} = \left(Y_0 \frac{Y_{\text{QPC}} + Y_0 \tanh((\alpha + i2\pi/\lambda)d_1)}{Y_0 + Y_{\text{QPC}} \tanh((\alpha + i2\pi/\lambda)d_1)} + Y_0 \frac{Y_d + Y_0 \tanh((\alpha + i2\pi/\lambda)d_2)}{Y_0 + Y_d \tanh((\alpha + i2\pi/\lambda)d_2)} \right)^{-1},$$

where Y_d is the admittance of the diode and α is the attenuation constant of the CPWG. The basic idea to match Z_L to $Z_0 = (Y_0)^{-1} = 50 \Omega$ is to choose d_1 such that for a certain frequency f the admittance of the load terminating the CPWG, in our case Y_{QPC} , is transformed to $Y_{d_1} = Y_0 + jB$ at the distance d_1 from the load. The susceptance B depends on Y_{QPC} . The length d_2 of the shunted stub is then designed such that the admittance of the stub is equal to $Y_{d_2} = -jB$ and hence the total admittance Y_L is exactly the characteristic admittance Y_0 .

For fixed $d_1 = 8.23 \text{ mm}$ and $d_2 = 8.47 \text{ mm}$, as in our case, the carrier frequency f and the capacitance of the varactor diode C_d are adjusted to achieve impedance matching ($Z_L = Z_0$ and hence $|\Gamma| = 0$). For distinct QPC conductance values, the reflection coefficient is measured as a function of the diode voltage V_d and the carrier frequency f , and pairs (f_m , $V_{d,m}$) can be extracted for which Z_L is closest to 50 Ω . In Fig. 1(c), the absolute value of the reflection coefficient $|\Gamma|$ versus frequency f for a fixed diode voltage is shown. The PCB is designed for a matching frequency close to 3 GHz, and we measure a full width at half maximum of around 100 MHz, which puts an upper limit on the setup bandwidth.

The samples are fabricated using photolithography and AFM lithography on a GaAs/AlGaAs heterostructure with a two-dimensional electron gas (2DEG) 34 nm below the surface. The 2DEG has a mobility of 33 m^2/Vs and an electron density of $4.8 \times 10^{15} \text{ m}^{-2}$ at a temperature of 4 K.

We compare 6 samples with 4 different designs shown in Figs. 2(a)–2(d). The mesas (darkest grey areas) are the conducting plateaus that remain after etching the GaAs/AlGaAs heterostructure. DC voltages are applied to the quantum structure via Ohmic contacts (white circles), including special rf Ohmic contacts (areas within dotted black lines) placed at different distances to the center mesa area, where a QPC is located. The rf Ohmic contacts in Figs. 2(c) and 2(d) are covered by 200 nm thick gold electrodes (light grey areas) forming CPWGs to optimize the rf performance. The CPWGs loss of about 30 dB/m is higher than the loss on the PCB but it is still not comparable to the resistive damping in the 2DEG.²¹ The inset of Fig. 2(c) shows the AFM scan of sample 4 including the AFM lines (red dotted line) forming the QPC.

In a charge detection measurement, charging a quantum dot (QD) by one electron causes a certain change in the QPC conductance. The maximum QPC conductance change due to one additional electron on the QD $|dg/dq|$ is a quantity that varies from one nanostructure to the next and is not a characteristic of the microscale chip design but depends on the nanostructure design. To measure the performance of the chip design, we therefore consider the change of the reflection coefficient for a given change in the QPC conductance

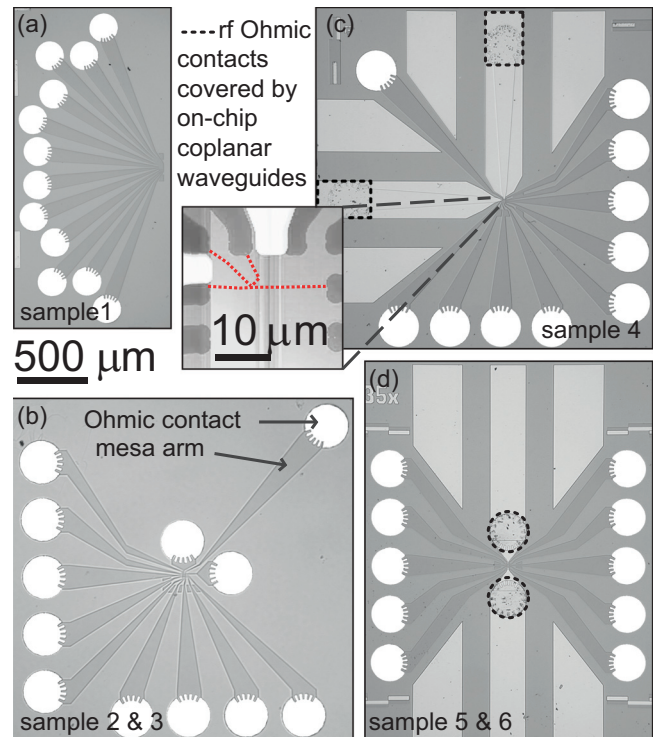


FIG. 2. Photographs of samples with the same design as (a) sample 1, (b) samples 2 and 3, (c) sample 4, and (d) samples 5 and 6. The white circles are conventional Ohmic contacts and the darkest grey areas are the mesa arms where the 2DEG remains after etching. In (c) and (d), the lightest grey areas are the coplanar waveguides where the thick dotted lines indicate additional Ohmic contacts. In the inset of (c), an AFM scan of the central mesa is shown and the fine red dotted line marks the AFM lithography oxide lines.

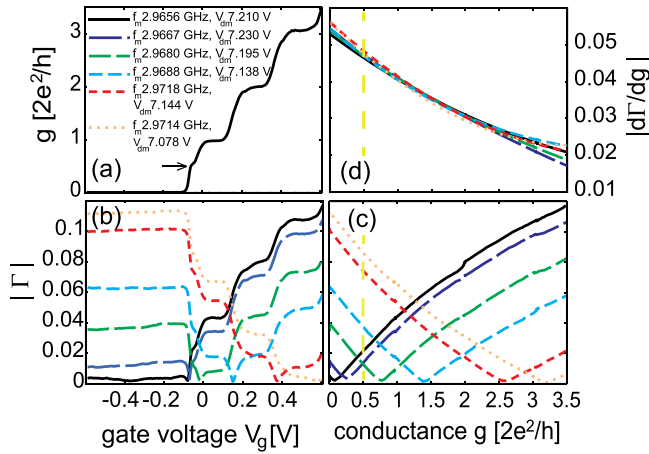


FIG. 3. (a) The dc conductance of the QPC as a function of gate voltage V_g . (b) The absolute value of the reflection coefficient $|\Gamma|$ depending on the gate voltage for different carrier frequencies f_m and different voltages V_{dm} applied to the diode. (c) $|\Gamma|$ as a function of the conductance obtained by combining the data of (a) and (b). (d) The derivative of Γ as a function of g . The dashed yellow line indicates the g value for which $|d\Gamma/dg|$ is the figure of merit for the sample.

$|d\Gamma/dg|$ by varying the voltage V_g on a gate electrode next to the QPC.²² The figure of merit for an optimized design is the slope $|d\Gamma/dg|$ of the curves evaluated at the conductance g where $|d\Gamma/dg| |dg/dq|$ has its maximum and this is usually close to $0.5 \times 2e^2/h$ as $|dg/dq|$ has a maximum there (arrow in Fig. 3(a)). Therefore, it is a good measure to compare $|d\Gamma/dg|$ at g equal to $0.5 \times 2e^2/h$ for different sample designs.

Fig. 3(a) shows the quantized conductance of the QPC as a function of gate voltage V_g .²³ A gate voltage independent contact resistance is subtracted from the measured resistance. These contact resistances were extracted to be between 1.2 and 4 k Ω for all samples except for samples 4a (9 k Ω) and 4b (15 k Ω).

We will now direct our attention to the rf measurements. The carrier signal power reaching the PCB is -65 dBm. The absolute value of the reflection coefficient $|\Gamma|$ is plotted as a function of QPC gate voltage for selected pairs (f_m , V_{dm}) in Fig. 3(b), where f_m is the matching frequency and V_{dm} is the diode voltage applied to achieve matching. The plateaus due to the quantized conductance of the QPC are clearly observable. By combining the data shown in Figs. 3(a) and 3(b), $|\Gamma|$ can be plotted as a function of conductance g (see Fig. 3(c)). In Fig. 3(d), the slope $|d\Gamma/dg|$ as a function of g is plotted.²⁴ It does not change significantly for curves with different matching points (conductance values for which $|\Gamma| = 0$ holds, corresponding to a pair (f_m , V_{dm})) from 0 to $3 \times 2e^2/h$ (see Fig. 3(d)). If the matching point is moved to even higher conductance values, a decrease in $|d\Gamma/dg|$ is expected for any g close to the pinch-off of the QPC.²⁵

Table I gives an overview of the main parameters of the 6 devices with the designs shown in Fig. 2. One characteristic is the distance between the QPC and the Ohmic contact through which the rf signal is applied. Long distances are $\geq 785 \mu\text{m}$ and short distances are $\leq 115 \mu\text{m}$. Half of the samples have a 50Ω on-chip CPWG which ends $\sim 10 \mu\text{m}$ before the QPC. Another criterion is the bonding. All samples are equipped with wedge bond wires (W, diameter $30 \mu\text{m}$) and

TABLE I. Characteristics of samples 1 to 6 including distance from the rf Ohmic contact to the QPC (long ($\geq 785 \mu\text{m}$) or short ($\leq 115 \mu\text{m}$)), on-chip coplanar waveguides (existent/inexistent) and wedge (W, samples 1-4a, 5, 6a) or ribbon (R, samples 4b, 6b) bonds to connect the samples to the PCB.

Sample no.	Distance		On-chip		Fig. 2
	to QPC		CPWG	Bonds	
1	$\sim 1000 \mu\text{m}$		No	W	(a)
2,3	$\sim 75 \mu\text{m}$		no	W	(b)
4a,4b	$\sim 785 \mu\text{m}$		yes	W,R	(c)
5	$\sim 115 \mu\text{m}$		yes	W	(d)
6a,6b	$\sim 110 \mu\text{m}$		yes	W,R	(d)

samples 4 and 6 additionally with ribbon bond wires (R, $100 \times 12 \mu\text{m}$ cross-sectional area, made out of Au).

The results are presented in Fig. 4 where $|d\Gamma/dg|_{g=0.5 \times 2e^2/h}$ is plotted for each sample for one representative pair (f_m , V_{dm}). It is clearly visible that all samples with on-chip CPWG (full squares/circles) perform better than the ones without on-chip CPWG (empty squares/circles), independent of the distance from the Ohmic contact to the QPC. A factor of 3 improvement from the standard sample (No. 1, distance $\geq 785 \mu\text{m}$, no on-chip CPWG) to the best sample (No. 5, distance $\leq 115 \mu\text{m}$, with on-chip CPWG) was achieved. For the samples without on-chip CPWG, the distance (long: red squares, short: black circles) over which the rf signal has to pass through the 2DEG before reaching the QPC seems to be a relevant criterion. One more sample supporting this result was measured, but as it was not possible to close the QPC to $0.5 \times 2e^2/h$ (due to leakage currents), the data are not shown here. The use of ribbon bonds for sample 4 shows an improvement compared to wedge bonds. All 6 curves measured at different matching points (same procedure as shown in Fig. 3) for sample 4b have a larger $|d\Gamma/dg|$ compared to all curves of sample 4a. However, for sample 6 no conclusion is possible as the on-chip CPWG was partly damaged during the bonding procedure. To check the reproducibility, samples 2 and 6b were cooled down

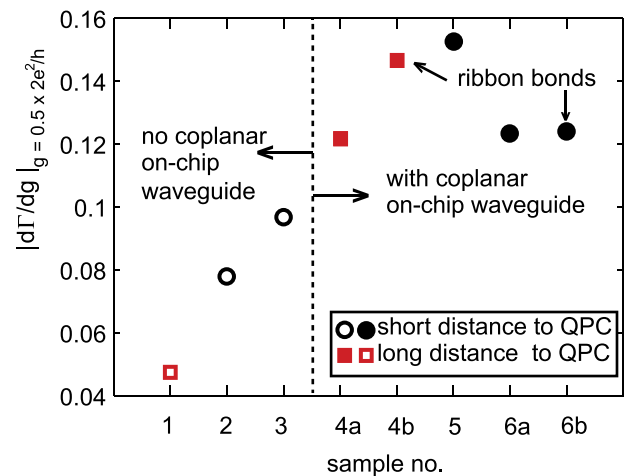


FIG. 4. $|d\Gamma/dg|_{g=0.5 \times 2e^2/h}$ for the 6 investigated samples. On-chip extensions of the coplanar waveguides (full squares/circles) increase the performance of the samples significantly. The distance from the Ohmic contact to the QPC (long: red squares, short: black circles) only plays a role in the samples without on-chip CPWG (empty squares/circles).

again, showing only small deviations. Furthermore, by moving to a different matching point, it was possible to improve the sensitivity by up to 11.5% at points not measured in the first cooldown.

In conclusion, we have presented an *in situ* tunable shunt stub matching circuit and observed that the sample chip design can be improved significantly leading to up to a factor of 3 improvement in $|d\Gamma/dg|_{g=0.5 \times 2e^2/h}$ by integrating coplanar waveguides into the design. A smaller improvement is achieved by simply reducing the distance between Ohmic contact and QPC. These designs can be adapted to other rf-matching circuits as well. The design of the matching circuit integrated into the PCB can be adjusted to higher resonance frequencies by decreasing the stub lengths accordingly. The tunability of the matching circuit facilitates impedance matching and the measurement of a variety of different samples in the future such as InAs nanowire or graphene quantum structures^{26,27} which are promising for an increased coupling between detector and nanostructure.

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¹⁹These transmission experiments compare coplanar waveguides where the waveguide is formed either by the not etched two-dimensional electron gas (2DEG) parts in a GaAs/AlGaAs heterostructure or by gold electrodes evaporated on top of a GaAs/AlGaAs heterostructure. The additional loss in the 2DEG was roughly 10 dB/mm for frequencies down to a few hundred MHz.
²⁰The reference plane is moved from the two cables connected to the VNA to the last SMA connector at RT and finally to the SMP connector to which the PCB is attached.
²¹P. J. Burke, I. B. Spielman, J. P. Eisenstein, L. N. Pfeiffer, and K. W. West, *Appl. Phys. Lett.* **76**(6), 745 (2000).
²²We assume that in future experiments amplitude and phase sensitive measurements can be performed.
²³All data shown in Fig. 3 were taken on sample 1.
²⁴The data are fitted with a cubic polynomial. The derivative of the fit is shown. The numerical derivation after averaging the data leads to the same but more noisy result.
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