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Influence of etching processes on electronic transport in mesoscopic InAs/GaSb quantum well devices

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We report the electronic characterization of mesoscopic Hall bar devices fabricated from coupled InAs/GaSb quantum wells sandwiched between AlSb barriers, an emerging candidate for two-dimensional topological insulators. The electronic width of the etched structures was determined from the low field magneto-resistance peak, a characteristic signature of partially diffusive boundary scattering in the ballistic limit. In case of dry-etching the electronic width was found to decrease with electron density. In contrast, for wet etched devices it stayed constant with density. Moreover, the boundary scattering was found to be more specular for wet-etched devices, which may be relevant for studying topological edge states. © *2015 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License.* [http://dx.doi.org/10.1063/1.4926385]

I. INTRODUCTION

Recently, InAs/GaSb composite quantum wells have gained a lot of interest due to the prediction of the quantum spin Hall (QSH) state in the inverted regime[1] of the bandstructure. In this state, transport is expected to be governed by counter propagating (helical) edge channels of opposite spins together with an insulating bulk and the system is referred to as a two-dimensional topological insulator (2D TI). The QSH state was first predicted[2] and observed[3] in HgTe/CdTe quantum wells. Electron-hole hybridization and the indication of a topological insulator phase were reported in InAs/GaSb quantum wells in recent transport experiments.[4–9] One important requirement to observe the 2D TI phase in electronic transport is to fabricate devices smaller than the inelastic scattering length (l_{in}). In reality, due to limited material quality often bulk transport is relevant and masks edge channel transport.[5] Moreover, edge scattering originating from rough edges as a result of fabrication processes, can also be detrimental to the observation of helical edge states.[10–12] Apart from being an emerging candidate for 2D TI, this system offers the potential to observe several physical phenomena such as exciton condensation,[13] Majorana Fermions,[14] or edge mode superconductivity.[15] In comparison to the HgTe/CdTe system, InAs/GaSb coupled quantum wells offer electric field tunability of the topological phase.[16]

When the device size becomes smaller than the elastic mean free path (l_e), the transport properties are modified with respect to bulk samples.[17–19] As a consequence mesoscopic devices exhibit enhanced resistivity due to the lateral boundary scattering, studied extensively in narrow channels fabricated in GaAs two-dimensional electron gases (2DEGs).[20,21] The electronic confinement in narrow 2DEGs depends a lot on the material system and particularly on the fabrication processes. For example, quasi-1D channels fabricated by reactive ion etching (RIE) in InAs 2DEGs[22] show a degradation of the mobility due to surface damage caused by the energetic ions along with lateral side wall depletion. Electronic transport in sub-micron devices of InAs[23] and InSb[24] based 2D systems were studied extensively. However, mesoscopic transport in InAs/GaSb systems is relatively unexplored. Compared to the pure InAs well, the presence of a GaSb layer may change the depletion width and the confinement potential. Hence, it is necessary to explore the mesoscopic properties of InAs/GaSb devices for reaching an optimized fabrication recipe.

Here, we present a detailed characterization of a series of mesoscopic Hall bar devices made by dry and wet etching processes (see Table I for details). The effective electronic width ($W_{electronic}$) was

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TABLE I. Details of the Hall bar devices: W_{etch} and L_{etch} are respectively the measured width and length between the voltage probes after etching. $W_{electronic}$ is the electronic width extracted from the measurements.

Device	Wafer	Etching type	Etching depth [nm]	W_{etch} [μm]	L_{etch} [μm]	$W_{electronic}$[a]	$\Delta R_L(B)/R_L(0)$[a]	Remark
D1	W1	Dry	300	2.0 ± 0.10	10.0	0.90	0.21	
D2	W1	Dry	300	4.1 ± 0.10	10.0	1.80	0.06	
D3	W1	Dry	300	25.0 ± 0.10	50.0	-	-	No detectable MR peak
D4	W3	Dry	300	2.1 ± 0.10	12.0	0.85	0.17	
D5	W3	Dry	300	4.1 ± 0.10	18.0	-	-	No detectable MR peak
D6	W2	Wet	200	1.9 ± 0.17	11.5	0.75	0.02	
D7	W2	Wet	350	2.6 ± 0.20	10.0	1.10	0.00	
D8	W2	Wet	350	4.4 ± 0.25	10.0	-	-	No detectable MR peak
D9	W3	Wet	1100	1.7 ± 0.42	10.0	0.45	0.06	
D10	W3	Wet	240	0.9 ± 0.12	11.0	0.46	0.01	
D11	W3	Wet	1600	22.2 ± 0.20	50.0	-	-	No detectable MR peak

[a]for $n \approx 9.5 \times 10^{11}$ cm^{-2}.

determined by measuring the low field magneto-resistance peak appearing due to partially diffusive boundary scattering.[17] We find that $W_{electronic}$ decreases with decreasing density for dry-etched devices, whereas it remains constant for wet-etched devices. The edge roughness in wet-etched devices was found to be smaller compared to dry-etched devices, which could be relevant for observing edge transport in this material.

II. FABRICATION

The devices were fabricated from wafers grown by molecular-beam epitaxy (MBE) with a similar growth structure as in Ref. 8. We present measurements on eleven Hall bar devices from three different wafers (W1, W2 and W3) with exactly the same nominal growth structure, but with different targeted lateral width. For the fabrication of the Hall bar devices, Ohmic contacts Ge(18 nm)/Au(50 nm)/Ni(40 nm)/Au(100 nm) and mesa were defined by optical lithography. For dry-etching, an Inductively Coupled Plasma (ICP) of Ar was used with a flow rate of 20 sccm. For wet etching we have used a phosphoric acid and the citric acid based III-V etchant, H_3PO_4:H_2O_2:$C_6H_8O_7$:H_2O (3 : 5 : 55 : 220) with a nominal etching rate of 10 – 15 nm/minute.[25] After etching, the devices are passivated with 200 nm of Silicon Nitride, deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) at ∼ 300 °C, which serves also as the dielectric for the top gate. Finally, the top gate is defined by one more step of optical lithography followed by the deposition of Ti/Au and lift-off. Figure 1(a) and 1(b) show the SEM images of typical dry-etched and wet-etched devices, respectively. Arrows in figure 1(b) indicate the measured length between the voltage probes (L_{etch}) and width (W_{etch}) after etching for the wet-etched device.

III. RESULTS AND DISCUSSION

We found all of our wafers to be electron doped at zero gate voltage with a density $n \approx 7 \times 10^{11}$ cm^{-2} irrespective of the fabrication processes. All the experiments were done by ac lock-in technique with a bias current of 10 – 50 nA and carrier frequency of 31 Hz at 1.3 K. Both electron and hole transport can be observed by tuning the gate voltage from positive to negative. Transport measurements on large Hall bars (25 μm × 50 μm) fabricated by both dry and wet etching possess similar carrier-mobilities and gate tunability as in Ref. 8.

Boundary scattering was characterized by measuring the longitudinal resistance (R_L) and its magnetic field dependence.[20] Figure 1(c) and 1(d) show typical low-field magneto-resistance (MR) data for dry and wet etched devices (devices D1 and D9 in Table I) at an electronic density, $n \approx 9.5 \times 10^{11}$ cm^{-2}. We find distinct MR peaks which are used to determine the electronic width

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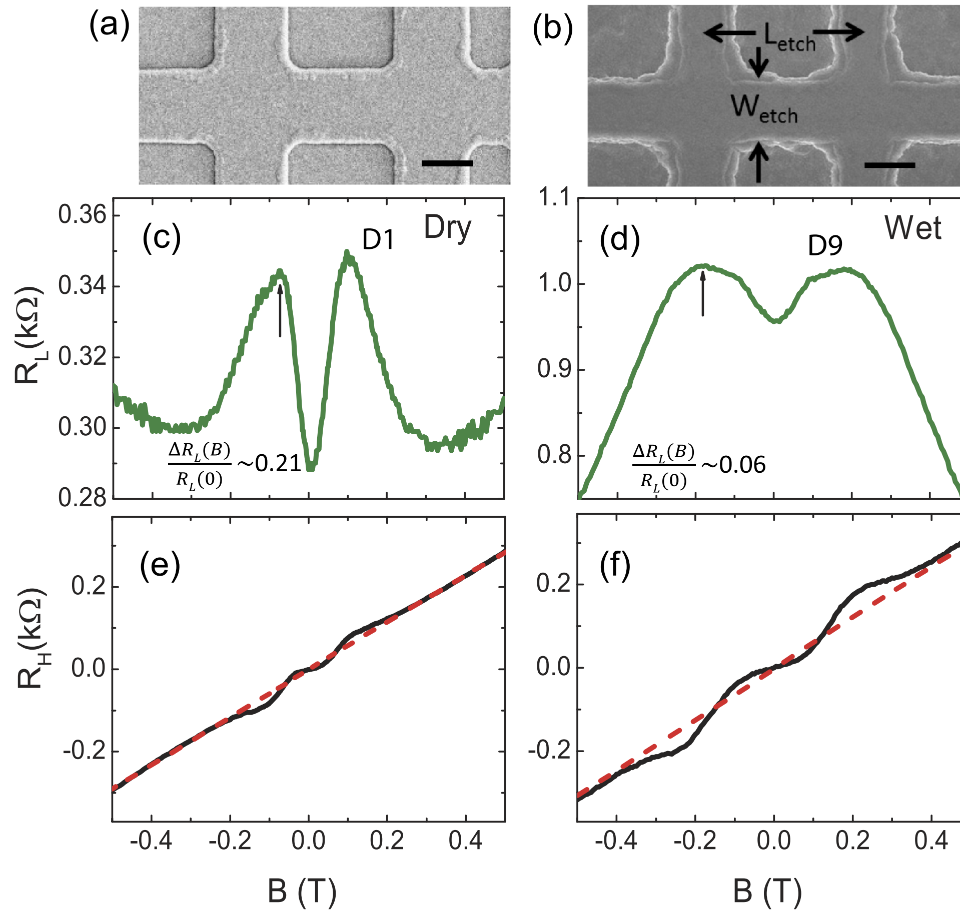

FIG. 1. SEM images of typical (a) dry and (b) wet-etched devices. Arrows in (b) indicate the length between the voltage probes (L_{etch}) and the width (W_{etch}) of the Hall bar after etching. Scale bar is 2 μm. (c)-(d) Longitudinal four-terminal resistance (R_{L}) and (e)-(f) (black solid lines) the Hall resistance (R_H), as a function of magnetic field (B) for devices D1 (dry-etched) and D9 (wet-etched), respectively, at a density $n \approx 9.5 \times 10^{11}$ cm^{-2}. The red dotted lines in (e) and (f) are $R_H - B$ curves at similar electronic density for wider devices, D3 (W=25 μm, dry-etched) and D11 (W=22.2 μm, wet-etched), respectively, indicating the absence of a quenched Hall effect near $B = 0$. The arrows in (c) and (d) indicate B_{max} (see text).

of the devices. When the device width becomes smaller than the elastic mean free path (l_e), charge carriers face partially diffusive boundary scattering in long channels ($L > l_{\text{e}}$). This results in a positive zero-field MR reaching a maximum at a field B_{max} (indicated by arrows in figure 1(c) and 1(d)) when the ratio of the wire width ($W_{\text{electronic}}$) and the cyclotron radius (R_c) follows the relation[17] $W_{\text{electronic}}/R_{\text{c}} = W_{\text{electronic}} e B_{\text{max}}/\hbar k_{\text{F}} = 0.55$, where $k_{\text{F}} = (2\pi n)^{1/2}$, is the Fermi wave vector. In the top left inset of figure 2(a), we compare l_e as a function of electronic density (n) for the three wafers (W1, W2 and W3), calculated from wider devices (D3, D8 and D11) where MR peaks were not observed. l_e was calculated using the relation, $l_e = h/\rho e^2 k_F$,[26] ρ being the measured resistivity.

Figure 1(e) and 1(f) (black solid lines) show the transverse MR (R_{H}) at $n \approx 9.5 \times 10^{11}$ cm^{-2} for devices D1 and D9, respectively, exhibiting quenching of the Hall resistance near zero field, a typical classical phenomenon of electron transport in ballistic crosses.[19,21] For wider devices the Hall effect becomes linear with magnetic field, indicated by the red dotted lines in figure 1(e) and 1(f), obtained from devices D3 (W=25 μm, dry-etched) and D11 (W=22.2 μm, wet-etched), respectively. Boundary scattering was observed mainly for high mobility electrons as l_{e} exceeds the device dimension only for densities larger than $\sim 7 \times 10^{11}$ cm^{-2}. No ballistic effects were observed for holes in this temperature range due to the low mobility and high effective mass. The roughness of the boundary can qualitatively be evaluated by calculating the quantity $\Delta R_{\text{L}}(B)/R_{\text{L}}(0)$,[20] where, $\Delta R_{\text{L}}(B) = R_{\text{L}}(B_{\text{max}}) - R_{\text{L}}(0)$, which is zero for completely specular boundary scattering. From

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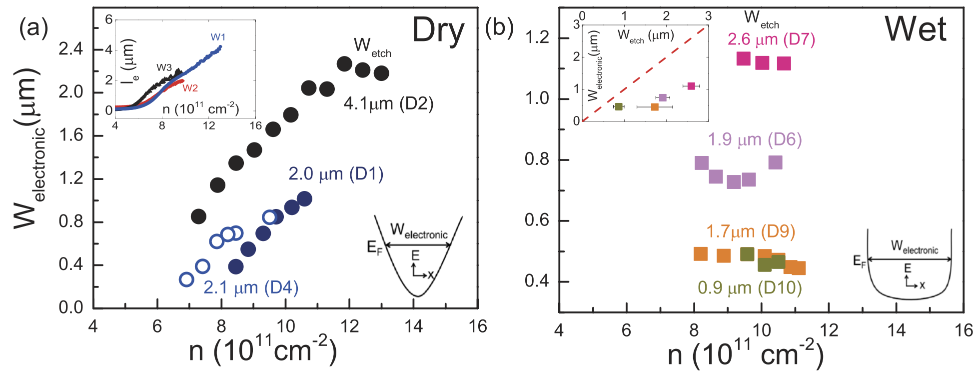

FIG. 2. The electronic width ($W_{electronic}$) is plotted as a function of density (n) for both (a) dry and (b) wet etched devices. The etched width (W_{etch}) and the corresponding device name are indicated for each devices. (Top left inset in a) Mean free path (l_e) is plotted as a function of density for three different wafers (W1, W2, W3). (Top left inset in b) Average $W_{\text{electronic}}$ is plotted against the mean etched width (W_{etch}) for wet-etched devices. The error bar indicates the uncertainty in measuring W_{etch}. The dashed line corresponds to $W_{\text{electronic}} = W_{\text{etch}}$. (Bottom insets) The electronic confinement potential for both etching processes is presented schematically.

figure 1(c) and 1(d), we see that $\Delta R_L(B)/R_L(0)$ is ~ 0.21 for device D1 and ~ 0.06 for device D9, confirming the smoother edge for the wet etched device (see Table I for other devices).

Next we concentrate on the density (n) dependence of the electronic width ($W_{\text{electronic}}$). Figure 2(a) shows the density dependence of three dry-etched devices (devices D1, D2, D4) with mean W_{etch} 2.0 μm, 4.1 μm and 2.1 μm, respectively. For all the three devices, $W_{\text{electronic}}$ was found to decrease with decreasing electron density. For device D2 ($W_{\text{etch}} \approx 4.1$ μm), $W_{\text{electronic}}$ saturates at around 2.2 μm above a density $n \approx 1.1 \times 10^{12}$ cm^{-2} and decreases to ≈ 0.8 μm at $n \approx 7.3 \times 10^{11}$ cm^{-2}, the lowest density where the MR peak was observed. Below this density the holes start populating the GaSb layer and transport is governed by both electrons and holes, where we see the signature of two band transport in both longitudinal and Hall resistance.[27] For devices D1 and D4 ($W_{\text{etch}} \approx 2.1$ μm), the saturation was not observed due to the limited gate range, however, a similar decrease in $W_{\text{electronic}}$ was observed. Figure 2(b) shows the density dependence of $W_{\text{electronic}}$ for all the wet-etched devices with a mean W_{etch} ranging between $0.9 - 2.6$ μm. For devices with $W_{\text{etch}} \approx 2.6$ μm (device D7) and ≈ 1.9 μm (device D6), $W_{\text{electronic}}$ was found to be 1.1 μm and 0.75 μm, respectively, with little variation with density. For devices D9 ($W_{\text{etch}} \approx 1.7$ μm) and D10 ($W_{\text{etch}} \approx 0.9$ μm), $W_{\text{electronic}}$ shows a similar value ~ 0.5 μm. Due to the larger etching depth for device D9 (≈ 1.1 μm) the side wall etching is expected to be more compared to device D10 (etching depth ≈ 240 nm) and may provide coincidentally similar $W_{\text{electronic}}$.

The density dependence of $W_{electronic}$ (figure 2) suggests a steeper confinement potential for wet-etched devices compared to the dry-etched ones (see insets of figure 2(a) and 2(b)), however, the exact shape of the confinement potential is difficult to model.

The depletion width is often used in literature to judge the quality of etching processes, defined as $W_{depletion} = 1/2(W_{\text{etch}} - W_{\text{electronic}})$. As $W_{\text{electronic}}$ varies with density for dry-etched devices, the depletion width is also not constant unlike for wet-etched devices, where $W_{\text{electronic}}$ remains constant with density. To get a reasonable comparison for the depletion width values, we have plotted average $W_{\text{electronic}}$ as a function of W_{etch} only for the wet-etched devices in the top inset of figure 2(b). The red dashed line indicates the line corresponding to $W_{\text{electronic}} = W_{\text{etch}}$. In wet etching we often find double step and corrugation at the edges due to the different etching rates for layers with different materials, in contrary to the dry etching where the etching is uniform (see figure 1(a) and 1(b)). This may lead to a larger uncertainty in determining the actual W_{etch} for the wet-etched devices. We find $W_{\text{depletion}}$ to be in the range $\sim 0.2 - 0.8$ μm, which is rather large compared to the pure InAs quantum well devices.[23] Moreover, the lateral depletion was found to increase for wider devices, which is counterintuitive. We also looked at the $W_{\text{depletion}}$ as a function of etching depth. However, no systematic dependence of $W_{\text{depletion}}$ with etching depth was observed in these four devices.

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Qualitatively, in these devices we found that the gate capacitance per unit area ($e.dn/dV_{TG}$) decreases for narrower devices. For a narrow channel with an ideal edge, one expects to have enhanced gate tunability due to the fringing field lines near the edge. We speculate that due to the etching process there could be depositions of non-volatile components, ionic charges *etc.*,.[28] These etchant residues may create charge traps near the edges which may be populated by the application of gate voltage. These trapped charges may screen the gate voltage, as well as modify the confinement potential in the lateral direction.

We plan to look into the influence of etching processes on the local and non-local electronic transport properties. Further work is necessary to reduce the bulk conduction either by improving the material quality or impurity doping[7] to observe the quantum spin Hall effect in this system.

IV. CONCLUSION

In conclusion, we have been able to fabricate and characterize mesoscopic devices of InAs/GaSb quantum well, made by two different etching processes. The electronic width was obtained from the low field magneto-resistance peak appearing due to boundary scattering. For dry-etched devices the electronic width decreases with lowering electron density, whereas, it remains constant for wet-etched devices. Our observations suggest that wet chemical etching is less invasive compared to the dry-etching and could be preferable to produce mesoscopic devices for studying topological insulators.

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