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Mapping leakage currents in a nanostructure fabricated via local anodic oxidation

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Abstract

The functionality of nanostructures fabricated via local anodic oxidation is limited by undesired leakage currents. We use low-temperature scanning gate microscopy to pin down the spatial position where leakage currents are most likely to occur. We show that leakage currents do not flow homogeneously along the complete barrier but at distinct weak points such as crossings of two oxide lines. These findings can be used to improve the design of such nanostructures.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The method of local anodic oxidation has proven to be useful to fabricate different nanostructures in silicon [1–4], metallic films [5–9] and two-dimensional electron gases (2DEGs) [10, 11]. Oxidation-based lithography has been used to define high-quality quantum point contacts [11, 12], quantum dots [11, 13], coupled quantum dots [14, 15], quantum rings [16–18] or combinations of these nanostructures [23, 19, 22] with high precision.

Despite the obvious opportunities offered by this technique one of its disadvantages is the occurrence of undesired leakage currents between different terminals of the structure beyond a threshold voltage of a few hundred millivolt. This limits the measurement range and therefore tuning options. Sometimes this eliminates the possibility to reach the desired measurement regime. In order to investigate a larger range of physical parameters, have a higher percentage of functional nanostructures and increase interpretability of the transport data, it is therefore crucial to fabricate nanostructures that do not show leakage currents.

These leakage currents are known to occur in all nanostructures fabricated with local anodic oxidation above a sample-dependent threshold voltage. However, little is known about the spatial distribution of these currents. If a leakage current flows between two adjacent terminals it is not known where this current flows or even if this current occurs homogeneously along the complete oxide line or rather at one particular point.

Scanning gate microscopy (SGM) enables us to investigate where leakage currents flow. When scanning a tip and recording a current map while a leakage current flows we are able to localize where leakage current is the strongest. Comparison with topography scans enables us to pinpoint at which point the current crosses the isolating oxide barrier allowing us to make a connection between the topological appearance of an oxide barrier and the most likely position where a leakage current will flow.

By making this connection we are able to pinpoint ‘weak’ points from the topography of atomic force microscopy (AFM)-written nanostructures. In the future this will help us to adjust the fabrication processes in a way to minimize leakage and therefore maximize tunability. This might give access to measurement ranges not accessible in the present samples.

2. Sample and setup

The wafer contains an AlGaAs–GaAs heterostructure with a 2DEG 34 nm below the surface. The 2DEG has a density of

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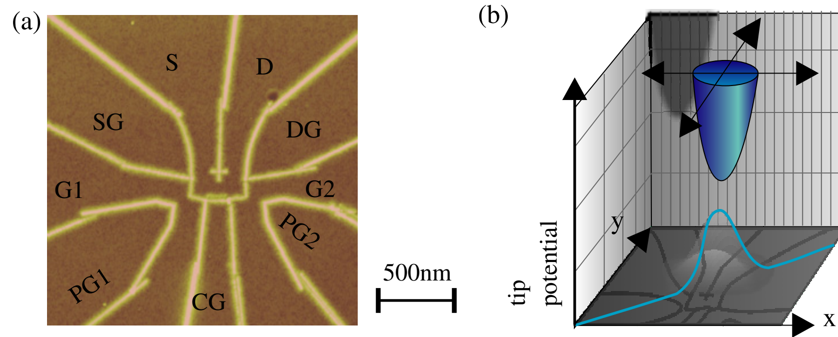

Figure 1. (a) AFM micrograph of the measured device. Regions above electrically conducting 2DEG regions are shown in darker brown. The isolating oxide lines appear as bright protrusions. The terminals are labeled with abbreviations that will be used to identify specific terminals of the structure. (b) Schematic representation of the principle of SGM.

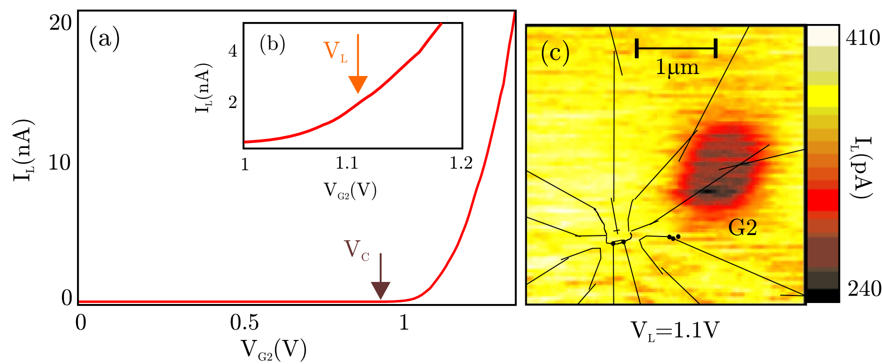

Figure 2. (a) Leakage current I_L versus the gate voltage V_{G2} applied to terminal G2. The leakage current rises linearly with voltage up to a critical break-through voltage (V_C) above which I_L rises exponentially with V_{G2}. (b) A zoom into (a) around the voltage V_L that is used to record the current map (c) of the leakage current from terminal G2. The oxide lines are drawn in black as guides to the eye.

$n_s = 5 \times 10^{15}$ m^{-2} and mobility of $\mu = 40$ m^2 V^{-1} s^{-1} at 4.2 K.

Oxide lines are produced via local anodic oxidation [10]. Using this method the 2DEG is depleted underneath an oxide line, forming an isolating barrier between two adjacent terminals. The oxide lines can be seen as white protrusions in figure 1(a).

In order to measure the leakage current between two terminals, a voltage is applied to the investigated terminal. All terminals that are not electrically connected to the terminal are grounded.

In SGM we use a metallic tip (wet etched PtIr wire mounted on a piezoelectric tuning fork sensor) to locally induce a repulsive tip potential in the sample as schematically shown in figure 1(b). The tip voltage is zero volt, which induces a finite tip induced potential in the sample as shown previously [21, 20]. We now investigate how the current flow changes when the tip potential is moved to different points of the sample, by recording so-called current maps. A current map displays the leakage current I_L in the structure versus the tip position. The tip–sample surface separation used for the measurements shown here is 31 nm.

All measurements are recorded in a ^{3}He cryostat with a measurement temperature around 300 mK.

3. Transport properties

No current should flow when applying a voltage to a single electrically isolated part of a structure defined by local anodic oxidation, while keeping the other, electrically isolated parts of the structure grounded. However, we observe that above a certain break-through voltage V_C a leakage current I_L flows from the investigated terminal G2 of the structure to other terminals of the structure, which should be electrically disconnected via potential barriers formed by the oxide lines (figure 2(a)). Above V_C the current rises approximately exponentially (figures 2(a) and (b)) with the applied voltage.

We observe a linear rise in current up to a break-through voltage of about $V_C = 0.995$ V. This current corresponds to a resistance of about 3 TΩ and is most likely limited by the leakage between cables in the cryostat. The finite current at zero applied voltage results from the offset of the I–V converter. The voltage V_L used to spatially investigate the leakage current is marked with the orange arrow.

4. Mapping of leakage currents

To determine the position where the leakage current flows across the oxide barrier we record current maps. Figure 2(c)

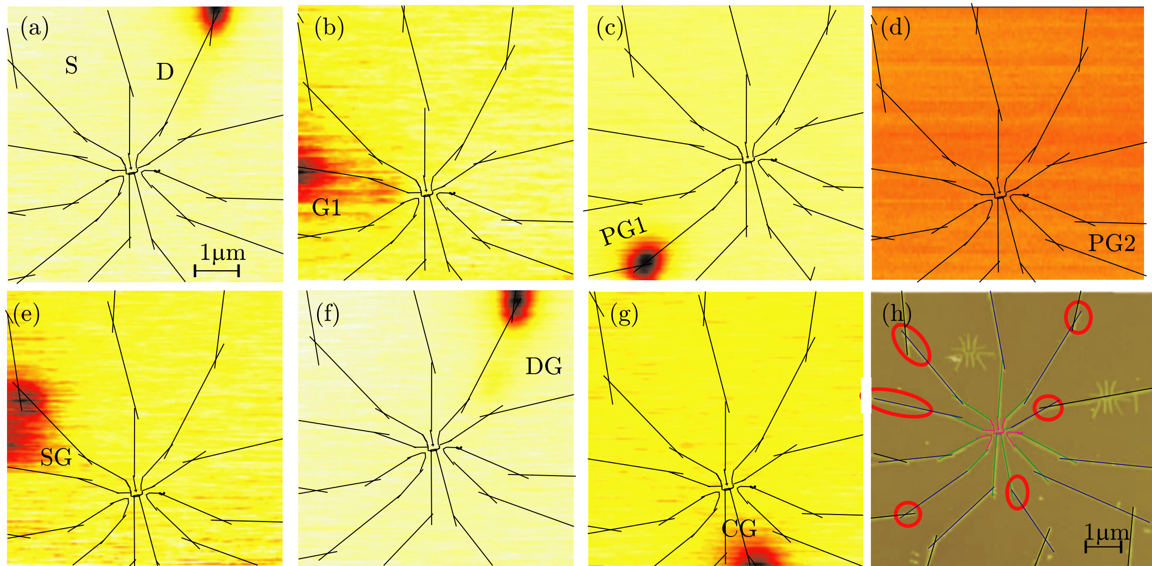

Figure 3. (a)–(h) Current maps for the leakage currents for all different terminals. The terminal to which the voltage was applied is labeled with the corresponding abbreviation. The black lines mark the positions of the oxide barriers. The color bars are adjusted for maximum visibility. (h) AFM-topography scan of the structure. The positions where leakage currents could be measured within the accessible scan frame are highlighted with red circles.

shows the current map for the leakage current that flows when applying V_L to terminal G2. We see that the current map is flat apart from a single region of suppressed current. For a circular region with a radius of about 300 nm the leakage current drops by a factor of two. This is the position where the leakage current crosses the oxide barrier. Leakage currents do not flow homogeneously along the complete extent of an oxide barrier, but rather cross the oxide barriers at a few 'weak' points. This is the typical behavior of spatially extended barriers fabricated in semiconductors and other materials.

We now mark the position of the oxide lines as determined right before the current map was recorded with black lines (figure 2(c)). The center of the region of suppressed current coincides with the topographical position where two oxide barriers cross.

Figures 3(a)–(g) shows analogous current maps for all terminals. We observe that for all terminals (except for terminal PG2 in panel (d) for which no leakage current position could be resolved within the accessible scan frame) the current maps display a single region of suppressed current. Below the break-through voltage V_C no leakage current is observed in the current maps. For voltages above V_C a leakage current can be observed as shown in figure 3, where the best visibility is found for voltages that are within a few hundred mV of V_C. This voltage is around 1 V for all terminals. When the applied voltage is set to larger values, leakage currents of several tenths of nA (not shown) can be observed. As the tip potential becomes comparatively small to the energy scale of the applied voltage, the features in the current maps become less pronounced for higher voltages. However, the position where the leakage current is found does not show any voltage dependence. The leakage current can flow across an oxide barrier in both directions. Here we localize the weakest point in the oxide barrier surrounding each terminal.

We now indicate all positions where we can determine leakage currents with red circles on a single topography scan as shown in figure 3(h). We observe one striking similarity: for five out of six positions we find that the 'weak' point in an oxide barrier is a crossing of two oxide lines.

The very nanostructure itself is robust against leakage currents. This area is usually written with a fresh tip and does not display any regions where two oxide lines overlap on a larger scale.

The favored occurrence of leakage currents at oxide line crossings can be explained as follows. When a first oxide line is written, it forms a pronounced oxide region (white lines in figure 1(b)). When forming the second oxide line, the AFM-tip is moved in feedback over the surface. When crossing the first oxide line, the effective writing distance from the tip to the 2DEG is larger than when writing a line on a 'fresh' part of the substrate, as the tip has to follow the 'hill' formed by the first oxide line. Due to this increased effective writing distance, the energy barrier of the second oxide line is weaker around the crossing. The lower energy barrier in this region makes it easier for charge carriers to cross it at this point. Thus it is likely that a leakage current will flow in the vicinity of an oxide line crossing.

The sample is produced in such a way that first the nanostructure up to the onset of the leads (pink in figure 3(h) online) is written. Then the first set of oxide lines (green online) from the nanostructure to the first crossing is written for all terminals. Afterward the lines between first and second crossing (blue online) are formed for all terminals and so on. At the positions of the innermost crossings the writing tip is still very sharp, allowing for a more pronounced and narrow oxide barrier. When writing the second crossing the tip has probably already degraded, presumably making those crossings prone to be the weak points within an oxide barrier. Therefore

leakage currents are less likely to occur at the very center of the nanostructure which is produced using a sharper tip.

In order to make nanostructures produced via local anodic oxidation more robust against leakage currents, crossings written with a blunt tip have to be avoided. One option is a 'hybrid' fabrication where part of the confining potential is formed via metallic gates [24]. In another approach, lines could be written without crossings, exchanging the tip for each new line forming a lead. Finally the nature of the crossings could be changed either by removing the ridge of the first line by etching before writing the second line or by adding many lines in parallel.

5. Conclusion

In conclusion, we have located the positions where leakage currents flow across oxide barriers. We observe that a leakage current does not flow uniformly across the oxide lines of a nanostructure along their whole length, but rather crosses the oxide barriers at distinct points. We show that leakage currents do not arise in the center of the nanostructure but rather at the leads. Crossings of two oxide lines are especially prone to the occurrence of leakage currents, due to the increased effective writing distance at those points during sample processing.

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